

IN THE CLAIMS

Please cancel claims 1-22 without prejudice.

Please amend claims 23-24 and 27-28 as follows below.

Please add new claims 29-37 that follow below.

The following is a listing of claims that will replace all prior versions, and listings, of claims in the application:

Listing of Marked Up Claims:

1 1- 22. (Cancelled).

1 23. (Currently Amended) A bipolar transistor,
2 comprising:
3 a substrate;
4 a base region having an intrinsic base region and an
5 extrinsic base region;
6 wherein the extrinsic base region is raised relative to
7 the intrinsic base region;
8 wherein the extrinsic base region has a thickness x and
9 the intrinsic base region has a thickness y , and wherein x
10 $[[>]]$ is greater than y .

1 24. (Currently Amended) The bipolar transistor of claim
2 23, further comprising an emitter structure, the emitter
3 structure comprising:
4 a polysilicon emitter having a first portion with a width
5 a , a second portion with a width b , and a third portion with a
6 width c ;

7 wherein $c > b$ is greater than $b > a$ which is greater
8 than a ; and
9 wherein the first portion defines an emitter base
10 junction, and wherein the third portion defines an emitter
11 contact region.

1 25. (Original) The bipolar transistor of claim 24,
2 wherein
3 the emitter region further comprises a nitride spacer
4 directly adjacent to the polysilicon emitter.

1 26. (Original) The bipolar transistor of claim 23,
2 wherein
3 the extrinsic base region comprises:
4 a first epitaxial layer; and
5 a second epitaxial layer on the first epitaxial
6 layer.

1 27. (Currently Amended) The bipolar transistor of claim
2 26, wherein
3 the first epitaxial layer is a SiGe epitaxial layer and
4 the second epitaxial layer is a heavily p-type doped Si
5 or SiGe epitaxial layer.

1 28. (Currently Amended) The bipolar transistor of claim
2 23, wherein
3 the bipolar transistor is being an npn transistor.

1 29. (New) A bipolar transistor, comprising:

2 a substrate having a collector region, the collector
3 region being a collector terminal;

4 a first epitaxial silicon layer on a surface of the
5 substrate;

6 an emitter stack on the first epitaxial silicon layer,
7 the emitter stack being an emitter terminal;

8 a second epitaxial silicon layer on portions of the first
9 epitaxial silicon layer located outside the emitter stack;

10 wherein a region of the first epitaxial silicon layer
11 located under the emitter stack is an intrinsic base region
12 and a region of the second epitaxial silicon layer on portions
13 of the first epitaxial silicon layer located outside the
14 emitter stack being a raised extrinsic base region;

15 wherein the raised extrinsic base region has a thickness
16 greater than a thickness of the intrinsic base region; and

17 wherein the intrinsic base region and the raised
18 extrinsic base region provide a base terminal of the bipolar
19 transistor with lower resistivity.

1 30. (New) The bipolar transistor of claim 29, wherein
2 the first epitaxial layer is a p-type Si, SiGe or SiGe:C
3 epitaxial layer and

4 the second epitaxial layer is a selectively deposited
5 heavily p-type doped Si epitaxial layer or a selectively
6 deposited heavily p-type doped SiGe epitaxial layer.

1 31. (New) The bipolar transistor of claim 29, wherein
2 the emitter stack includes

3 a first oxide layer on the first epitaxial silicon
4 layer;

5 a first nitride layer on the first oxide layer;

6 a second oxide layer on the first nitride layer;
7 ions implanted through an emitter window in the
8 second oxide layer and the first nitride layer to form a
9 polysilicon emitter.

1 32. (New) The bipolar transistor of claim 29, wherein
2 the bipolar transistor is a Si, SiGe or SiGe:C npn
3 bipolar transistor.

1 33. (New) A bipolar transistor having a base, a
2 collector, and an emitter, the bipolar transistor comprising:
3 a substrate with a collector region;
4 a base region coupled to the substrate, the base region
5 having an intrinsic base region and an extrinsic base region;
6 a polysilicon emitter structure coupled to the intrinsic
7 base region; and
8 wherein the extrinsic base region has a thickness X and
9 the intrinsic base region has a thickness y , and wherein X is
10 greater than Y .

1 34. (New) The bipolar transistor of claim 33, wherein
2 the extrinsic base region is raised relative to the
3 intrinsic base region.

1 35. (New) The bipolar transistor of claim 33, wherein
2 the polysilicon emitter structure has a first portion
3 providing an emitter base junction, a second portion providing
4 conduction, and a third portion providing an emitter contact
5 region.

1 36. (New) The bipolar transistor of claim 35, wherein
2 the first portion of the polysilicon emitter structure
3 has a width A,
4 the second portion of the polysilicon emitter structure
5 has a width B differing from A,
6 the third portion of the polysilicon emitter structure
7 has a width C differing from A and C.

8 37. (New) The bipolar transistor of claim 36, wherein
9 the width C is greater than the width B which is greater
10 than the width A.